(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 487 302 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
05.06.1996 Bulletin 1996/23

(51) Int Cl.[6]: **G01N 27/92**, C30B 33/00, C30B 33/08

(21) Application number: **91310648.0**

(22) Date of filing: **19.11.1991**

(54) Method for testing electrical properties of silicon single crystal

Verfahren zur Feststellung der elektrischen Eigenschaften eines Silizium-Monokristalles

Méthode pour tester les propriétés électriques d'un monocristal de silicium

(84) Designated Contracting States:
DE FR GB

(30) Priority: **22.11.1990 JP 320467/90**

(43) Date of publication of application:
27.05.1992 Bulletin 1992/22

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Printed by Jouve, 75001 PARIS (FR)

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Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

This invention relates to a method for testing electrical properties of a silicon single crystal and more particularly to a method for evaluating dielectric breakdown voltage of the silicon oxide film grown on the surface of a polished wafer derived from the Czochralski(CZ) method or the floating zone (FZ) method by subjecting the single crystal derived therefrom to chemical treatments and visual inspection.

DESCRIPTION OF THE PRIOR ART

Heretofore, as means for evaluating the quality of a silicon semiconductor single crystal rod which has been pulled up by the Czochralski method or the floating zone pulling method, the so-called evaluation of oxide film dielectric breakdown voltage which comprises preparing a silicon polished wafer (PW wafer) from the single crystal rod, causing the silicon wafer to form an oxide film on the surface thereof, attaching a polysilicon electrode to the silicon wafer, applying a bias voltage thereto, and determining the dielectric breakdown voltage of the oxide film has been practised. This method has been recognized as one of the important. testing techniques because it permits substantially equivalent simulation of the formation of a device on a silicon wafer and allows determination of the question as to whether or not the wafer manifests a suitable quality during the manufacture of a device using the wafer.

The evaluation of oxide film dielectric breakdown voltage mentioned above, however, entails such problems as (1) inability to effect this evaluation until after the PW wafer has been prepared, (2) inevitable consumption of enormous time during the process of evaluation, and (3) necessitation of an expensive apparatus for evaluation, for example.

This invention has as an object thereof the provision of a method which is capable of quickly and inexpensively effecting equivalent evaluation of the oxide film dielectric breakdown voltage of a wafer cut out of a given grown semiconductor single crystal without requiring prepararion of a PW wafer for the evaluation.

The other objects and characteristic features of the present invention will become apparent to those skilled in the art as the disclosure is made in the following description of a preferred embodiment of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sketch diagram of scale-like patterns formed on the surface of a silicon wafer when the silicon wafer has been subjected to mirror etching and then to etching with a SECCO solution, Fig 2 is a graph showing the density of scale-like patterns formed on the surface of a CZ silicon wafer when the silicon wafer has been subjected to mirror etching and then to etching with a SECCO solution (SECCO etch pit density) as a function of the rate of pulling the crystal, and Fig 3 is a graph showing the density of scale-like patterns formed on the surface of a CZ silicon wafer when the CZ silicon wafer has been subjected to mirror etching and then to etching with a SECCO solution (SECCO etch pit density) as a function of the acceptability rate of oxide film dielectric breakdown voltage %.

SUMMARY OF THE INVENTION

The objects described above are accomplished by this invention providing a method for testing electrical properties of a silicon single crystal, characterised by pulling up a silicon semiconductor single crystal by a Czochralski method or the floating zone pulling method, cutting a wafer of a prescribed thickness from said single crystal, etching the surface of the wafer with a mixed solution of hydrofluoric acid and nitric acid thereby relieving said wafer of strain, then setting the wafer upright in a mixed solution of $K_2Cr_2O_7$, hydrofluoric acid and water and selectively etching the surface of the wafer therein for a period in the range from 10 to 60 minutes, and taking count of the number of scale-like patterns consequently appearing on the surface of the wafer, thereby evaluating the oxide film dielectric breakdown voltage of said silicon single crystal.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

For the evaluation by the method described above, the wafer is desired to have a thickness not less than 0.3 mm and not more than 2 mm. In order for the surface of this wafer to be smoothly and flatly etched, the ratio of hydrofluoric acid to nitric acid in the mixed solution is desired to be approximately 1:3. The selective etching of the wafer in the mixed solution of $K_2Cr_2O_7$, hydrofluoric acid, and water is desired to be carried out by keeping the wafer immersed in the mixed solution at normal room temperature for a period in the range of from 10 to 60 minutes.

As the mixed solution of $K_2CR_2O_7$, hydrofluoric acid, and wafer, the SECCO solution [F. Secco D'Aragona: "J. Electrochem. Soc., Vol. 119, No. 7 (1972), pp. 948-951] has found popular recognition. The composition of the SECCO solution is obtained by dissolving $K_2CR_2O_7$ in a proportion of 0.15 mol in water and mixing the resultant aqueous solution with an aqueous 49% hydrofluoric acid solution to a volumetric ratio of 1:2. The SECCO solution has been used for the purpose of selectively etching a heat-treated OSF (oxidation induced stacking fault) thereby producing a line defect image or for the purpose of visualising a slippage suffered to oc-

cur in an ingot during the growth of the ingot. The use of this SECCO solution in visualizing scale-like patterns on a wafer as contemplated by this invention has never been known to the art.

The production of scale-like patterns is accomplished by cutting a wafer from a grown silicon semiconductor single crystal rod, subjecting the surface of the wafer to mirror etching with the mixed solution of hydrofluoric acid and nitric acid, and then further subjecting the resultant mirror surface of the wafer to etching with the mixed solution of $K_2Cr_2O_7$, hydrofluoric acid, and water. One example of a surface forming such scale-like patterns is illustrated in Fig. 1. A deliberate observation of this surface under an optical microscope reveals the presence of a minute pit 2 at the peak of each scale-like pattern 1. These scale-like patterns 1 are liable to generate such a gas as hydrogen at the portions of the pits 2. They occur as signs of uneven etching when the gas escapes upwardly. This fact is evinced by the phenomenon that these scale-like patterns are expanded upwardly in the vertical direction when the wafer is set upright in the liquid. It is inferred, however, that the scale-like patterns originate in a certain kind of crystalline defect inherent in a crystal. The scale-like patterns formed by the etching of the wafer cut from the grown silicon semiconductor single crystal rod with the mixed solution of $K_2Cr_2O_7$, hydrofluoric acid, and water are found by examination to possess a density difference. This density difference is satisfactorily correlated with the oxide film dielectric breakdown voltage which is determined of a plurality of PW wafers. This fact established the method of this invention to be capable of effecting an evaluation equivalent to the evaluation of the oxide film dielectric breakdown voltage of a PW wafer prepared from the single crystal rod.

The evaluation of the oxide film dielectric breakdown voltage of a silicon semiconductor single crystal is carried out by cutting a wafer out of the single crystal rod immediately after its growth, etching the surface of the wafer with the mixed solution of hydrofluoric acid and nitric acid thereby relieving the wafer of strain, then etching the surface of the wafer with the mixed solution of $K_2Cr_2O_7$, hydrofluoric acid, and water thereby inducing occurrence of pits and scale-like patterns on the surface, determining the density of the scale-like patterns, and computing the oxide film dielectric breakdown voltage by making use of the correlation between the density of scale-like patterns and the oxide film dielectric breakdown voltage.

Examples

Now, the present invention will be described more specifically below with respect to working examples.

A plurality of silicon semiconductor single crystal rods 130 mm in diameter were pulled up, some by the CZ method and others by the FZ method. In the case of the CZ method, a quartz crucible 45 cm in diameter was used and the material placed therein was doped with boron and adjusted to an electric resistance coefficient of 10 Ω cm. In all the single crystal rods pulled up by this method, the orientation was invariably <100>. In pulling up the silicon semiconductor single crystal rods by the case of the CZ method, the speed of pulling was varied from one batch to another between 0.4mm/min to 1.7 mm/min. Incidentally, it is well known that the desirability of the oxide film dielectric breakdown voltage decreases in accordance as the pulling speed increases.

From each of the silicon single crystal rods produced by the pulling, silicon wafers 1 mm in thickness were sliced with a diamond saw and used as test pieces. Such a silicon wafer was subjected to mirror etching with the aforementioned mixed solution of hydrofluoric acid and nitric acid, washed thoroughly with purified water, and subjected to selective etching with the SECCO solution for a period in the range of from 1 to 60 minutes. On the test pieces etched for periods exceeding 10 minutes, scale-like patterns illustrated in Fig. 1 were observed extending upwardly in the vertical direction which the wafers were set upright in the solution. On the test pieces etched for periods exceeding 60 minutes, the formed scale-like patterns overlapped and consequently defied efforts in taking count of the density thereof. The wafer etched with the aforementioned liquid for 30 minutes, a period empirically found to be just fit, was placed under an optical microscope for the operator to take count of the density of scale-like patterns. The data of density thus obtained were plotted on a graph as a function of the speed of crystal growth. The results are shown in Fig.2. In Fig.2, the count of scale-like patterns was represented in the SECCO pit density. It is clearly noted from the graph that the SECCO pit density increased in accordance as the speed of crystal growth increased.

From the CZ silicon semiconductor single crystal rods mentioned above, PW wafers were prepared. The surfaces of these PW wafers were etched similarly with the SECCO solution and tested for SECCO etch pit density. The density distribution consequently obtained of these wafers was equal to that obtained of the wafers prepared from the aforementioned grown single crystal rods. This fact establishes the method of this invention to be capable of measuring the SECCO etch pit density without requiring the subsequent preparation of PW wafers.

For the purpose of investigating the correlation between the SECCO etch pit density of such a wafer and the oxide film dielectric breakdown voltage, the PW wafers were subjected to a heat treatment in preparation for determination of the oxide film dielectric breakdown voltage. The wafers resulting from the heat treatment were cleaned with a RCA detergent and then subjected to gate oxidation at 900°C for 100 minutes to form an oxide film 25 nm in thickness. On the oxide film-coated wafers, polysilicon was deposited and phosphorus was diffused to form an electrode pattern 8 mm^2 in area. For

the measurement of the dielectric breakdown voltage of the oxide film, a voltage was applied to form an electric field of several MV/cm between the electrode and the silicon substrate. The level of voltage at which an electric current of not less than 1 mA/cm^2 began to flow was defined as the dielectric breakdown voltage. The wafers exhibiting not less than 8 MV/cm of oxide film dielectric breakdown voltage were rated as non-rejectable. The proportion nonrejectable was obtained by dividing the number of nonrejectable chips found in one PW wafer by the total number of chips formed in the same PW wafer and multiplying the quotient by 100. Fig.3 shows the SECCO etch pit density as a function of the proportion nonrejectable represented in oxide film dielectric breakdown voltage (%). The two magnitudes involved herein showed a clear correlation such that the desirability of the oxide film dielectric breakdown voltage decreases in accordance as the SECCO etch pit density increased.

When wafers taken from the FZ silicon semiconductor single crystal rod were subjected to the same test, it was found that entirely the same correlation existed between the SECCO etch pit density and the oxide film dielectric breakdown voltage. In accordance with the method of this invention, therefore, the oxide film dielectric breakdown voltage property of a grown silicon semiconductor single crystal rod for the SECCO etch pit density without necessitating preparation of PW wafers and subsequent evaluation of the oxide film dielectric breakdown voltage thereof. This fact proves the effectiveness of this invention in the evaluation of interest.

In accordance with the present invention, a silicon semiconductor single crystal rod grown from molten silion by the Czochralski method or the floating zone method can be given an evaluation equivalent to the evaluation of the oxide film dielectric breakdown voltage, one of the electrical properties, of a silicon wafer simply by cutting a wafer of a prescribed thickness from the single crystal rod instead of elaborately preparing silicon polished wafers from the single crystal rod, etching the surface of the wafer with the mixed solution of hydrofluoric acid and nitric acid thereby relieving the wafer of strain, then etching the surface with the mixed solution of $K_2Cr_2O_7$, hydrofluoric acid, and water for a prescribed length of time, and taking count of scale-like patterns consequently produced on the surface. This invention, therefore, obviates the necessity for spending time and labor in the preparation of the polished wafer, alloting time to the attendant step for evaluation, and installing an expensive device for evaluation and permits an evaluation equivalent to the evaluation of the oxide film dielectric breakdown voltage to be carried out quickly and inexpensively the use of a wafer cut out of the grown silicon semiconductor single crystal rod.

Claims

1. A method for testing electrical properties of a silicon single crystal, characterized by pulling up a silicon semiconductor single crystal by the Czochralski method or the floating zone pulling method, cutting a wafer of a prescribed thickness from said single crystal, etching the surface of the wafer with a mixed solution of hydrofluoric acid and nitric acid thereby relieving said wafer of strain, then setting the wafer upright in a mixed solution of $K_2Cr_2O_7$, hydrofluoric acid and water and selectively etching the surface of the wafer therein for a period in the range from 10 to 60 minutes, and taking count of the number of scale-like patterns consequently appearing on the surface of the wafer, thereby evaluating the oxide film dielectric breakdown voltage of said silicon single crystal.

Patentansprüche

1. Verfahren zum Testen der elektrischen Eigenschaften eines ' Siliziumeinkristalls, gekennzeichnet durch ein Hochziehen eines Halbleiter-Siliziumeinkristalls durch das Czochralski-Verfahren oder das Flottierzone-Ziehverfahren, Abschneiden eines Wafers einer vorgeschriebenen Dicke von dem Einkristall, Ätzen der Oberfläche des Wafers mit einer Mischlösung aus Fluorwasserstoffsäure und Salpetersäure, um dadurch das Wafer von einer Belastung frei zu machen, anschließendes Aufstellen des Wafers aufrecht in einer Mischlösung aus $K_2Cr_2O_7$, Fluorwasserstoffsäure und Wasser und selektives Ätzen der Oberfläche des Wafers in derselben für eine Dauer in dem Bereich von 10 bis 60 Minuten und Zählung der Anzahl von schuppenförmigen Mustern, die danach auf der Oberfläche des Wafers erscheinen, um dadurch die bielektrische Oxidfilm-Überschlagspannung des Siliziumeinkristalls auszuwerten.

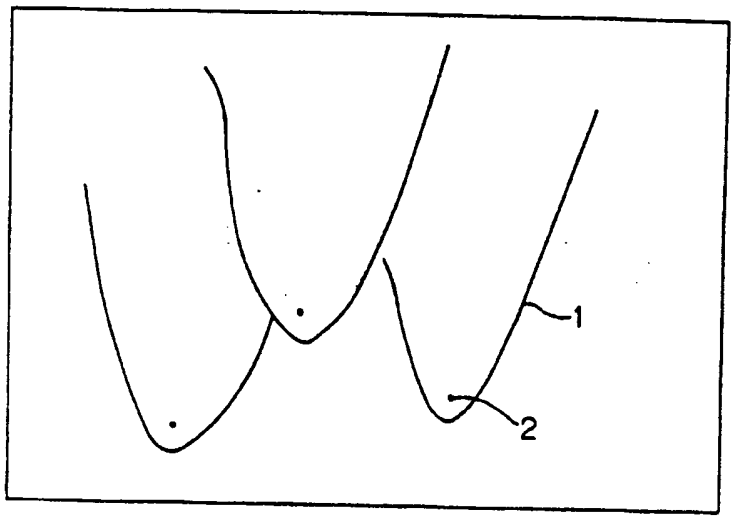
Revendications

1. Méthode pour contrôler les propriétés électriques d'un monocristal de silicium, caractérisée en que :
   - on réalise un monocristal de silicium semiconducteur par la méthode de Czochralski ou la méthode de la zone flottante,
   - on découpe une galette d'épaisseur déterminée dudit monocristal,
   - on grave la surface de la galette par application d'une solution d'acide fluorhydrique et d'acide nitrique pour dégager ladite galette des contraintes,
   - ensuite, on place verticalement la galette dans une solution de $K_2Cr_2O_7$, d'acide fluorhydrique et d'eau,
   - puis on grave selectivement la surface de la ga-

lette au sein de cette solution pendant des périodes de durée comprises entre 10 et 60 minutes,

- enfin, on compte le nombre de motifs en forme de dépôt apparaissant à la surface de la galette pour ainsi évaluer la tension diélectrique de claquage du film d'oxyde dudit monocristal de silicium.

FIG.1



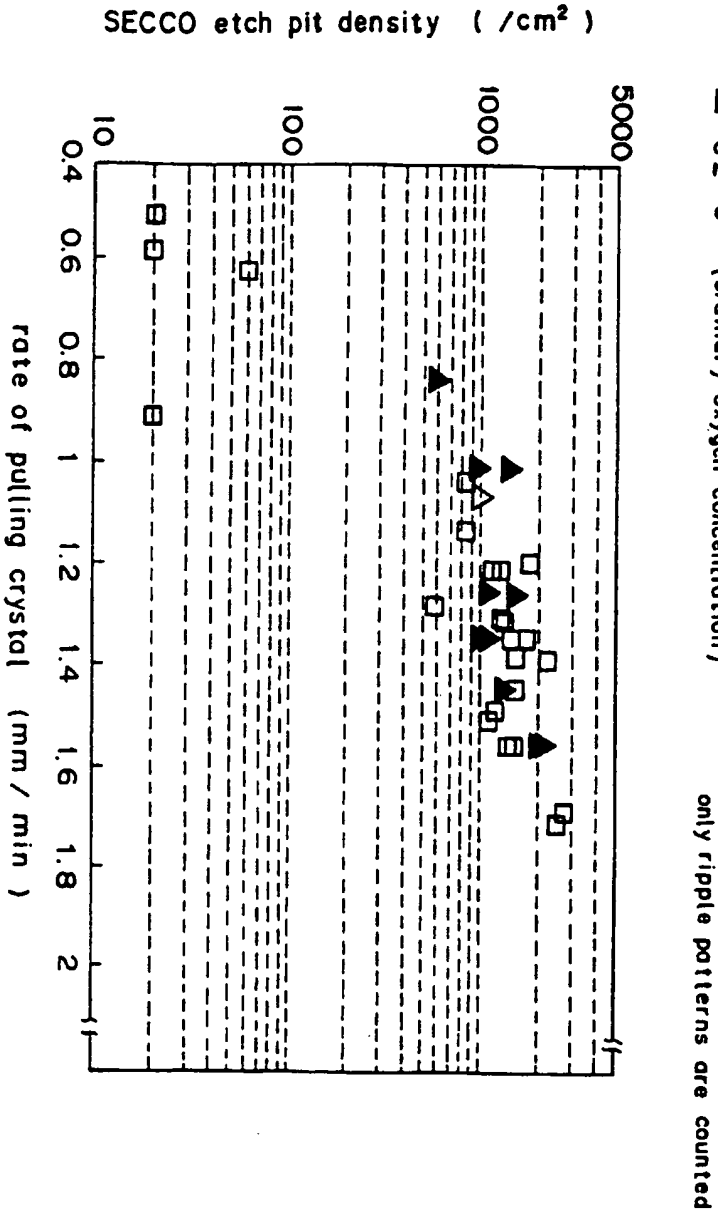

SECCO etch pit density (/cm²)
5000
1000
100
10
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
rate of pulling crystal (mm / min)
Sample
□ CZ 5" (low oxygen concentration)
Δ CZ 5" (ordinary oxygen concentration)
▲ CZ 5" (ordinary oxygen concentration)
Condition
rate of pulling crystal:
average in 10cm
test piece etched for 30 minutes:
only ripple patterns are counted

FIG.2

FIG. 3

Sample

□ CZ 5" (low oxygen concentration)

▲ CZ 5" (ordinary oxygen concentration)

Condition

oxide film dielectric breakdown voltage:
gate area = 8 mm²
judging current of polysilicon gate = 1mA/cm²
oxidation condition:
900℃ 100minutes (dry O_2)
film thickness = 250Å
criterion for judging:
acceptability rate = %
(> 8MV/cm²)